EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Applicant Attorney Roger Fulghum on June 6, 2008.

The application has been amended as follows:

- Claim 1, replace with -- A method for managing power consumption in a computer system having a processor, comprising the steps of: providing an array of redundant power supplies, wherein each power supply in the array of redundant power supplies is rated to a power delivery capacity that is less than a maximum power draw of the computer system; identifying by an array controller a loss of operation of a power supply of the array of redundant power supplies, wherein a total rated capacity of functioning power supplies of the array of redundant power supplies is less than the maximum power draw of the computer system; and reducing an operating speed of the processor of the computer system. --.
- Claim 4, replace with -- The method for managing power consumption in a computer system of claim 1, wherein the step of identifying the loss of operation of the power supply of the array of redundant power supplies comprises the step of notifying a BIOS of the computer system of the loss of operation of the power supply of the array of redundant power supplies. --.

- Claim 5, replace with -- The method for managing power consumption in a computer system of claim 4, wherein a signal at the processor is asserted by the BIOS of the computer system. --.
- Claim 6, replace with -- The method for managing power consumption in a computer system of claim 1, further comprising the step of increasing the operating speed of the processor in conjunction with operation of all power supplies of the array of redundant power supplies. --.
- Claim 7, replace with -- A computer system, comprising: an array of redundant power supplies, wherein each power supply of the array is rated to a power delivery capacity that is less than a maximum power draw of the computer system; and a processor; wherein an operating speed of the processor is reduced upon a loss of a power supply of the array of redundant power supplies, wherein the loss is identified by an array controller, whereby a power draw of the computer system is reduced to a level below a total rated capacity of functioning power supplies of the array, and wherein the total rated capacity of the functioning power supplies of the array is less than the maximum power draw of the computer system. --.
- Claim 8, replace with -- The computer system of claim 7, wherein the operating speed of the processor is reduced by an assertion of a signal at the processor to cause the processor to enter a system management mode. --.

- Claim 10, replace with -- The computer system of claim 7, wherein the array of redundant power supplies includes the array controller for identifying a failure or a removal of the power supply of the array of redundant power supplies. --.
- Claim 11, replace with -- The computer system of claim 7, further comprising a BIOS for receiving an indication of the loss of the power supply and for asserting a signal to cause the processor to reduce a clock speed of a clock in the processor. --.
- Claim 13, replace with -- The computer system of claim 7, further comprising a BIOS for receiving an indication of the loss of the power supply and for asserting a signal to cause a lower voltage level to be applied to the processor. --.
- Claim 14, replace with -- The computer system of claim 7, further comprising a BIOS for receiving an indication of the loss of the power supply and for asserting a signal to reduce a data rate of a front side bus of the processor. --.
- Cancel claims 15-19.
- Claim 20, replace with -- A method for reducing a power draw of a computer system having an array of redundant power supplies, wherein each power supply is rated to a power delivery capacity that is less than a maximum power draw of the computer system, comprising the steps of: identifying by an array controller a loss of a power supply of the computer system, wherein a total rated capacity of functioning power supplies of the array is less than the maximum power draw of the computer system; determining whether the power draw of the computer system has reached or exceeded a predetermined threshold level; and causing a

processor to enter a power conservation state when the power draw of the computer system reaches or exceeds the threshold level. --.

- Claim 21, replace with -- The method for reducing the power draw of a computer system of claim 20, wherein the step of causing the processor to enter the power conservation state comprises the step of causing the processor to reduce an effective rate of at least one internal clock of the processor. --.
- Claim 24, replace with -- The method for reducing the power draw of a computer system of claim 20, wherein the step of causing the processor to enter the power conservation state comprises the step of lowering a data rate of a front side bus of the processor. --.

2. The following is an examiner's statement of reasons for allowance: the claims are allowable because none of the prior art(s) cited, anticipate(s) or render(s) obvious a method of claim 1, with "… identifying by an array controller a loss of operation of a power supply of the array of redundant power supplies, wherein a total rated capacity of functioning power supplies of the array of redundant power supplies is less than the maximum power draw of the computer system…" in conjunction -- i.e., viewed as a whole -- with the other limitations of the claim; a computer system of claim 7, with "… wherein an operating speed of the processor is reduced upon a loss of a power supply of the array of redundant power supplies… whereby a power draw of the computer system is reduced to a level below a total rated capacity of functioning power supplies of the array… wherein the total rated capacity of the functioning power supplies of the array is less than the maximum power draw of the computer system" in conjunction -- i.e., viewed as a whole -- with the other limitations of the claim; a method of claim 20, with "…

identifying by an array controller a loss of a power supply of the computer system, wherein a total rated capacity of functioning power supplies of the array is less than the maximum power draw of the computer system..." in conjunction -- i.e., viewed as a whole -- with the other limitations of the claim.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to TSE CHEN whose telephone number is (571)272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tse Chen/
Primary Examiner, Art Unit 2116
June 9, 2008